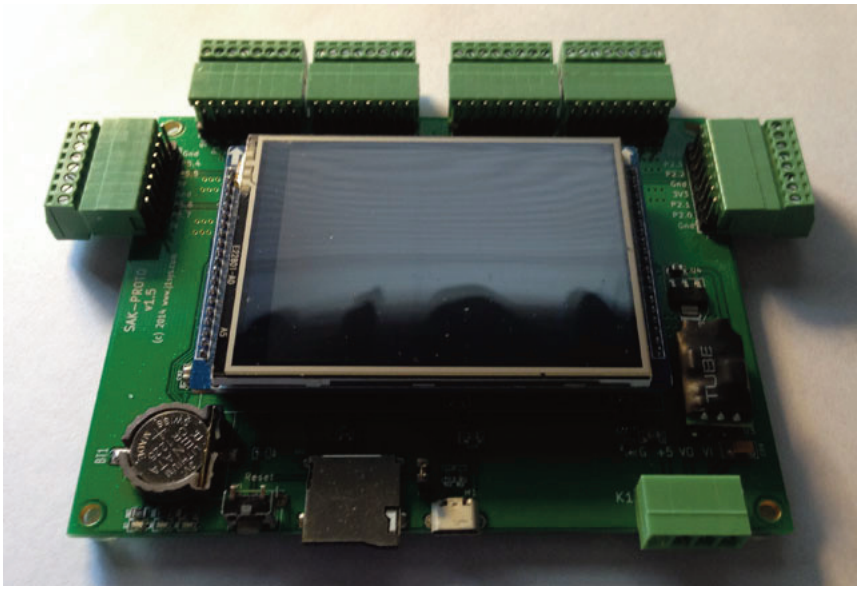
SAK-PROTO Product Datasheet

v1.5



Features

- PSoC 5LP CY8C5268AXI-LP047 Processor
- 3.3V HY28B 2.8” 320x240 RGB LCD w/Touch
- microUSB, microSD, reset, status LEDs, Qty 10 3.3V user I/O, Qty 12 5V user I/O
- Versatile power supply options

General Description

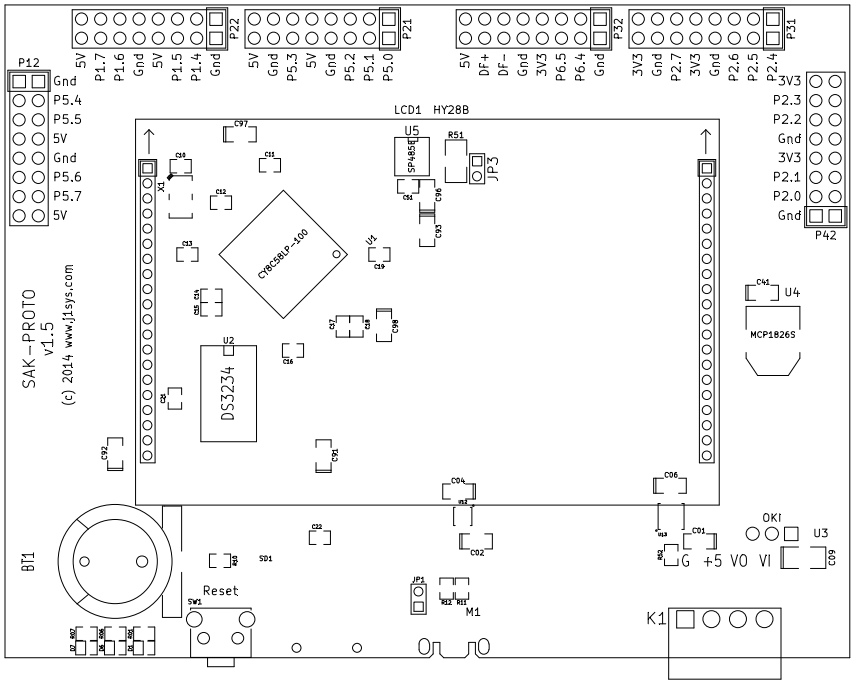
Our initial SAK board is the SAK-PROTO development board. It includes a PSoC 5LP 100pin TQFP processor, a battery backed up DS3234 RTC, a 5V RS485 transceiver, a 3.3V HY28B 2.8" 320x240 RGB LCD w/Touch, microUSB, microSD, reset, versatile power configurations, Qty 10 3.3V I/O signals and Qty 12 5V I/O signals brought out to pluggable 2.54mm screw terminal connectors on the board edges.

The board comes preloaded with our versatile Universal Boot Loader (j1UBL) that allows for firmware updates over the microUSB using our extended j1UBL Host or the stock Cypress Bootloader Host, or firmware updates loaded from the microSD card.

Using PSoC's versatile I/O pin placement most of the pins can be reallocated to the users digital I/O.

Analog I/O functions may be limited by the PSoC's normal restrictions.

Board Layout



Jumpers

Jumper	Description
JP1	This jumper will connect the ID signal from the microUSB to the Reset line of the PSoC5LP. Normally should be installed. Must be installed to program the board with a new bootloader or other non-bootloadable hex file using an SWD programmer. May be remove if you are concerned with users connecting a 5 wire microUSB cable and accidently reseting the device.
JP3	This jumper will enable the 120ohm terminating resistor across the RS485 signal pair. Normally should be installed. Can be removed if this unit will be in the middle of an RS485 bus.

Connectors

Connector	Description
M1	microUSB for SWD programming, bootloader communications, or application USB usage. Can also supply 5VDC for board operation.
K1	Flexible DC power connector. The board can work on 5VDC or 7VDC-40VDC based on K1 wiring. Please see power options section.
CAUTION - P12,P12,P22,P31,P32,P42 use various pinouts with Ground and +V on different/conflicting pins. Please take care to use the proper connections to avoid short circuiting the power supply.	
P12, P21, P22	5VDC Power and I/O Pins. Each connector has 4 signals, 2 ground, 2 +5VDC. Note: P12 and P22 have the same pinout, P21 has a unique pinout.
P32	Mixed use 5VDC RS485 and 3.3VDC I/O Pins.
P31, P42	3.3VDC Power and I/O Pins. P32 has the same pinout of P12 and P22 with 3.3V voltage and signals. P31 has the same pinout of P21 with 3.3V voltage and signals.

M1 is a microUSB socket, K1 is a 3.5mm pluggable screw terminal, all Pxx connectors have both a 2.54mm pluggable screw terminal and a 1x8 2.54mm header adjacent to the connector.

M1 microUSB Connector	
Pin	**Description**
1	USB VBus. 5VDC
2	D-, SWDCK
3	D+, SWDIO
4	USB ID, Used for Reset for SWD if jumper JP1 is installed
5	Ground

K1 Flexible DC Power Connector There are 3 power options. 5VDC can be supplied via M1, 5VDC can be supplied by K1, or 7VDC-40VDC can be supplied to K1 and 5VDC from the DC-DC converter supplied to the board. An automatic load switches between the microUSB (M1) power and the external power (K1). The external power (K1) takes precedence.	
Pin	**Description**
1	Ground
2	5VDC Power Input to board
3	5VDC Power Output from DC-DC converter (connect to pin 2 if using DC-DC converter)
4	7VDC - 40VDC Power Input to DC-DC converter

P12 5VDC Input/Output Connector	
Pin	**Description**
1	Ground
2	P5[4], GPIO - 5VDC I/O
3	P5[5], GPIO - 5VDC I/O
4	5VDC
5	Ground
6	P5[6], GPIO - 5VDC I/O
7	P5[7], GPIO - 5VDC I/O
8	5VDC

P21 5VDC Input/Output Connector	
Pin	**Description**
1	P5[0], GPIO - 5VDC I/O
2	P5[1], GPIO - 5VDC I/O
3	P5[2], GPIO - 5VDC I/O
4	Ground
5	5VDC
6	P5[3], GPIO - 5VDC I/O
7	Ground
8	5VDC

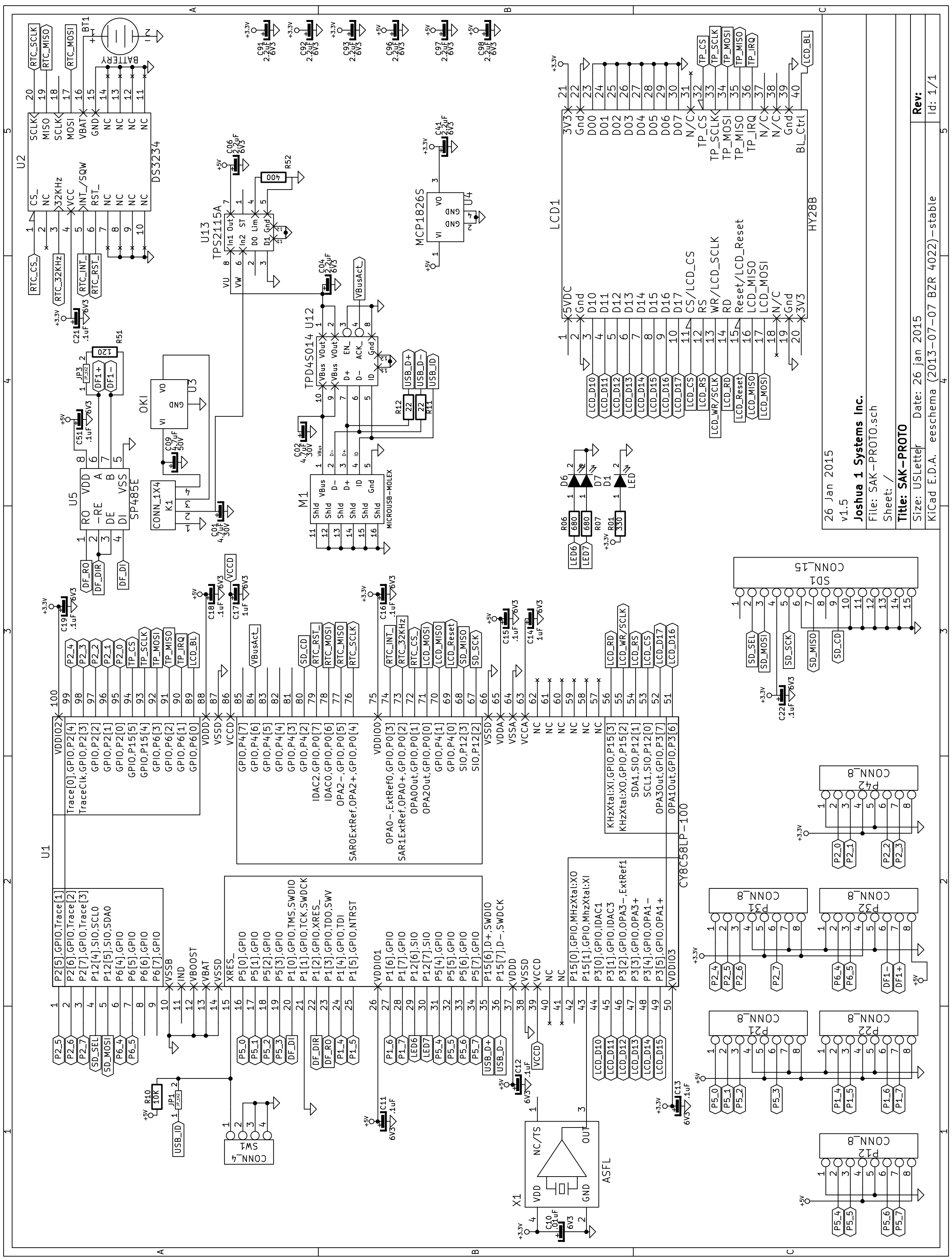
P22 5VDC Input/Output Connector	
Pin	**Description**
1	Ground
2	P1[4], GPIO - 5VDC I/O
3	P1[5], GPIO - 5VDC I/O
4	5VDC
5	Ground
6	P1[6], GPIO - 5VDC I/O
7	P1[7], GPIO - 5VDC I/O
8	5VDC

P31 3.3VDC Input/Output Connector	
Pin	**Description**
1	P2[4], GPIO - 3.3VDC I/O
2	P2[5], GPIO - 3.3VDC I/O
3	P2[6], GPIO - 3.3VDC I/O
4	Ground
5	3.3VDC
6	P2[7], GPIO - 3.3VDC I/O
7	Ground
8	3.3VDC

P32 5VDC/3.3VDC Mixed Input/Output Connector	
Pin	**Description**
1	Ground
2	P6[4], GPIO - 3.3VDC I/O
3	P6[5], GPIO - 3.3VDC I/O
4	3.3VDC
5	Ground
6	DF- RS485 5VDC Differential
7	DF+ RS485 5VDC Differential
8	5VDC

P42 3.3VDC Input/Output Connector	
Pin	**Description**
1	Ground
2	P2[0], GPIO - 3.3VDC I/O
3	P2[1], GPIO - 3.3VDC I/O
4	3.3VDC
5	Ground
6	P2[2], GPIO - 3.3VDC I/O
7	P2[3], GPIO - 3.3VDC I/O
8	3.3VDC

Schematic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Joshua 1 Systems Inc.
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Size: USLetter Date: 26 jan 2015
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Rev:
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U1
CY8C58LP-100
U2
DS3234
U5
SP485E
U12
TPD4S014
U13
TPS2115A
U4
MCP1826S
U3
OKI
M1
MICROUSB-MOLEX
LCD1
HY28B
BT1
BATTERY
X1
ASFL
SD1
CONN_15
SW1
CONN_4
K1
CONN_1X4

SWD Programming

The user can design and compile any stand-alone or custom bootloader project. The output of the compilation process will be a HEX file compatible with miniProg 3 or most other SWD programmers. If the user wants to install the project on SAK-PROTO then they can use the supplied 5pin to microUSB cable to program the device. JP1 should be installed. The SWD programmer should be set for 5VDC operation and should supply power to the board. Even if external power is connected (which will take precedence) the power must be supplied so that the programmer will detect the 5VDC. The microUSB does NOT output 5VDC on the VBus pin.

j1UBL Bootloader Operation

SAK-PROTO is supplied with an installed j1UBL bootloader or the user can install the HEX file for the bootloader with an SWD programmer (see above). The user can use this bootloader to install bootloadable CYACD applications without an SWD program. The application can be uploaded using Cypress's Bootloader Host, our j1UBL application on a Windows PC, or from a microSD card inserted into the microSD card socket.

On reset the bootloader will initialize the HY28B if enabled. It will then display an informational screen.

The bootloader will check for a FAT32 formatted microSD card. If present it will check for a /boot directory. If present it will check for a CYACD file (first found). If present it will compare the IDs with the currently installed app. If they match it will check the date/time of the CYACD file against the installed app. If either the IDs or date/time are different it will then install the app. Progress of the above checks and the installation of the app will be displayed on the HY28B if enabled.

If any of the above checks and searches for a CYACD file on a microSD card fail or if the current application matches the found CYACD file the bootloader will wait upto 8 seconds for a connection from a bootloader host via a USB connection. If the connection is made the bootloader will remain in bootloader mode until commanded to proceed by the bootloader host.

After 8 seconds with no connection the bootloader will start the installed application if present.

All of the above may appear laborious and overkill but we found that if the user left the microSD in place with a bootloadable CYACD file present then the bootloader would re-install the firmware on each boot. The above sequence of events will protect against that but still allow a developer to test iterative versions of a work in process without having to take care to update the App IDs each time.

j1UBL Bootloadable Recommended Configuration

j1UBL in its full configuration currently consumes approximately 26KB of Flash. By default the bootloadable component will place your application starting at the next flash block boundary. We recommend setting the application starting point manually and setting the start address to 32KB (0x8000). This will allow for upgrades to the bootloader without having to rebuild all bootloadable projects.

Bootloadable Settings	
Name	**Value**
Application Version	user defined
Application ID	user defined
Application Custom ID	user defined
Application Image Start Address	0x8000
Application Image End Address	0x3FEFF
Manual Application Image Placement	True

You will need to link the supplied HEX and ELF files with your bootloadable project. The Cypress linker requires that many of the system settings must match between the bootloader and bootloadable.

System Configuration Settings	
Name	**Value**
Device Comfiguration Mode	Compressed
Enable Error Correcting Code (ECC)	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	user defined
Stack Size (bytes)	user defined
Include CMSIS Core Peripheral Library Files	True

Ports and Pin Assignments

The following pins of the PSoC5LP are assigned to onboard peripherals and I/O ports:

HY28B Pins				
Name	**Description**	**Port**	**Pin**	**Type**
LCD_D10-LCD_D17	LCD Parallel Bus for Communication	P3[0:7]	44-49, 51,52	Software I/O, 3v3
LCD_CS	LCD Chip Select	P12[0]	53	Digital Out, 3v3
LCD_RD	LCD Read	P15[3]	56	Digital Out, 3v3
LCD_WR	LCD Write (SCLK)	P15[2]	55	Digital Out, 3v3
LCD_RS	LCD Register Select	P12[1]	54	Digital Out, 3v3
LCD_Reset	LCD Reset	P4[0]	69	Digital Out, 3v3
LCD_MISO	LCD Master In Slave Out	P4[1]	70	Digital In, 3v3
LCD_MOSI	LCD Master Out Slave In	P0[0]	71	Digital Out, 3v3
TP_CS	Touch Panel Chip Select	P15[5]	94	Digital Out, 3v3
TP_SCLK	Touch Panel SPI Clock	P15[4]	93	Digital Out, 3v3
TP_MOSI	Touch Panel Master Out Slave In	P6[3]	92	Digital Out, 3v3
TP_MISO	Touch Panel Master In Slave Out	P6[2]	91	Digital In, 3v3
TP_IRQ	Touch Panel Touch Active (IRQ)	P6[1]	90	Digital In, 3v3
LCD_BL	LCD Backlight	P6[0]	89	Digital Out, 3v3

microSD Pins				
Name	**Description**	**Port**	**Pin**	**Type**
SD_SEL	microSD Select	P12[4]	4	Digital Out, 3v3
SD_SCK	microSD SPI Clock	P12[2]	67	Digital Out, 3v3
SD_MOSI	microSD Master Out Slave In	P12[5]	5	Digital Out, 3v3
SD_MISO	microSD Master In Slave Out	P12[3]	68	Digital In, 3v3
SD_CD	microSD Card Detect	P4[2]	80	Digital In, 3v3

LED Indicator Pins				
Name	**Description**	**Port**	**Pin**	**Type**
LED6	LED Indicator D6	P12[6]	29	Digital Out, 5v
LED7	LED Indicator D7	P12[7]	30	Digital Out, 5v

Real Time Clock Pins				
Name	**Description**	**Port**	**Pin**	**Type**
RTC_CS	RTC Select	P0[1]	72	Digital Out, 3v3
RTC_SCK	RTC SPI Clock	P0[4]	76	Digital Out, 3v3
RTC_MOSI	RTC Master Out Slave In	P0[6]	78	Digital Out, 3v3
RTC_MISO	RTC Master In Slave Out	P0[5]	77	Digital In, 3v3
RTC_32KHz	RTC 32KHz Clock Output	P4[2]	80	Digital In, 3v3
RTC_INT_	RTC Interrupt	P0[3]	74	Digital In, 3v3
RTC_RST_	RTC Reset	P0[7]	79	Digital In, 3v3

USB/SWD Pins				
Name	**Description**	**Port**	**Pin**	**Type**
USB_D+	USB D+, SWDIO	P15[6]	35	Digital I/O, 5v
USB_D-	USB D-, SWDCK	P0[4]	36	Digital I/O, 5v
VBusAct_	VBus Active (Not)	P0[6]	78	Digital Out, 3v3

RS485 Pins				
Name	**Description**	**Port**	**Pin**	**Type**
DF_RO	RS485 Receiver Output	P1[3]	23	Digital In, 5v
DF_DIR	RS485 Direction	P1[2]	22	Digital Out, 5v
DF_DI	RS485 Driver Input	P1[0]	20	Digital Out, 5v

P12 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P5_4	P12 Connector I/O Pin 2	P5[4]	31	User Defined, 5v
P5_5	P12 Connector I/O Pin 3	P5[5]	32	User Defined, 5v
P5_6	P12 Connector I/O Pin 6	P5[6]	32	User Defined, 5v
P5_7	P12 Connector I/O Pin 7	P5[7]	34	User Defined, 5v

P21 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P5_0	P21 Connector I/O Pin 1	P5[0]	16	User Defined, 5v
P5_1	P21 Connector I/O Pin 2	P5[1]	17	User Defined, 5v
P5_2	P21 Connector I/O Pin 3	P5[2]	18	User Defined, 5v
P5_3	P21 Connector I/O Pin 6	P5[3]	19	User Defined, 5v

P22 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P1_4	P22 Connector I/O Pin 2	P1[4]	24	User Defined, 5v
P1_5	P22 Connector I/O Pin 3	P1[5]	25	User Defined, 5v
P1_6	P22 Connector I/O Pin 6	P1[6]	27	User Defined, 5v
P1_7	P22 Connector I/O Pin 7	P1[7]	28	User Defined, 5v

P31 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P2_4	P31 Connector I/O Pin 1	P2[4]	99	User Defined, 3v3
P2_5	P31 Connector I/O Pin 2	P2[5]	1	User Defined, 3v3
P2_6	P31 Connector I/O Pin 3	P2[6]	2	User Defined, 3v3
P2_7	P31 Connector I/O Pin 6	P2[7]	3	User Defined, 3v3

P32 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P6_4	P32 Connector I/O Pin 2	P6[4]	6	User Defined, 3v3
P6_5	P32 Connector I/O Pin 3	P6[5]	7	User Defined, 3v3

P42 Connector I/O Pins				
Name	**Description**	**Port**	**Pin**	**Type**
P2_0	P42 Connector I/O Pin 2	P2[0]	95	User Defined, 3v3
P2_1	P42 Connector I/O Pin 3	P2[1]	96	User Defined, 3v3
P2_2	P42 Connector I/O Pin 6	P2[2]	97	User Defined, 3v3
P2_3	P42 Connector I/O Pin 7	P2[3]	98	User Defined, 3v3